CLAIMS:

1. A host-fabric adapter, comprising:

at least one Micro-Engine (ME) arranged to establish connections and support data transfers, via a switched fabric, in response to work requests from a host system for data transfers;

a context memory interface arranged to provide context information necessary for data transfers; and

a doorbell manager arranged to update the context information needed for said Micro-Engine (ME) to process said work requests for data transfers, via said switched fabric.

2. The host-fabric adapter as claimed in claim 1, wherein said context memory interface comprises:

an address translator arranged to perform the address translation between a ME assigned address and a memory physical address to access context information; and

a context memory having a bandwidth optimized, vertically sliced memory architecture arranged to store context information needed for said Micro-Engine (ME) to process said work requests for data transfers, via said switched fabric.

3. The host-fabric adapter as claimed in claim 2, wherein said context memory contains a large quantities of context registers arranged to store context information needed for said Micro-Engine (ME) to process said work requests for data transfers.

4. The host-fabric adapter as claimed in claim 3, wherein said Micro-Engine (ME), said context memory interface, and said doorbell manager are configured in accordance with the "*Virtual Interface (VI) Architecture Specification*", the *"Next Generation Input/Output (NGIO) Specification"* and the *"InfiniBand*^{TM} *Specification"*.

5. The host-fabric adapter as claimed in claim 2, wherein said context memory having a bandwidth optimized, vertically sliced memory architecture is partitioned vertically into multiple memory slices based on a register width requirement, each of which supplies respective bits of data of a predetermined register width to said Miro-Engine (ME), via a system bus of said predetermined register width, and a number of registers of each of said multiple memory slices corresponds to a designated number needed by network device requirements.

6. The host-fabric adapter as claimed in claim 2, wherein said Micro-Engine (ME), said context memory interface, and said doorbell manager are implemented as part of an Application Specific Integrated Circuit (ASIC).

7. The host-fabric adapter as claimed in claim 2, wherein said context memory having a bandwidth optimized, vertically sliced memory architecture is partitioned vertically into multiple memory slices based on a register width requirement, each of said memory slices contains registers corresponding to a total number of registers of a designated size provided by data network requirements, each of said memory slices has a register width selected to supply respective bits of data to said Micro-Engine (ME), via a system bus of a predetermined register width, and a register depth selected to correspond to the total number of registers of said designated size, and all of said memory slices except for a last memory slice contain a respective default location initialized to zero which serves as a padding value to said system bus of said predetermined register width, when the respective last memory location of said memory slices is accessed by said Micro-Engine.

8. The host-fabric adapter as claimed in claim 2, wherein, when a register width requirement is 32 bits, and a system architecture requires 15 registers of 8 bits, 8 registers of 12 bits, and 17 registers of 32 bits for a total of 40 registers, said context memory having a bandwidth optimized, vertically sliced memory architecture is partitioned into three memory slices, including Memory A of 40x8 registers arranged to supply first 8 bits of 32-bit data, via a system bus of 32 bits, Memory B of 25x4 registers arranged to supply next 4 bits of 32-bit data, via said system bus of 32 bits, and Memory Z of 17x20 registers arranged to supply last 20 bits of 32-bit data, via said system bus of 32 bits, wherein said Memory B and Memory Z each contains

an additional default, last memory location initialized to zero which serves as a padding value to said system bus of 32 bits, when the respective default, last memory location of a respective memory slice is accessed by said Micro-Engine.

9. The host-fabric adapter as claimed in claim 2, wherein, when a register width requirement is 32 bits and a system architecture requires 5 registers of 8 bits, 10 registers of 12 bits, 15 registers of 24 bits and 20 registers of 32 bits for a total of 50 registers, said context memory having a bandwidth optimized, vertically sliced memory architecture is partitioned into four memory slices, including Memory A of 50x8 registers arranged to supply first 8 bits of 32-bit data, via a system bus of 32 bits, Memory B of 45x4 registers arranged to supply next 4 bits of 32-bit data, via said system bus of 32 bits, Memory C of 35x12 registers arranged to supply next 12 bits of 32-bit data, and Memory Z of 20x8 registers arranged to supply last 8 bits of 32-bit data, via said system bus of 32-bits, wherein said Memory C, Memory B and Memory Z each contains an additional default, last memory location initialized to zero which serves as a padding value to said system bus of 32 bits, when the respective default, last memory location of a respective memory slice is accessed by said Micro-Engine.

10. A host-fabric adapter installed at a host system for connecting to a switched fabric of a data network, comprising:

at least one Micro-Engine (ME) arranged to establish connections and support data transfers via said switched fabric;

a serial interface arranged to receive and transmit data packets from said switched fabric for data transfers;

a host interface arranged to receive and transmit host data transfer requests, in the form of descriptors, from said host system for data transfers;

a context memory having a bandwidth-optimized, area-minimal vertically sliced memory architecture arranged to store context information needed for said Micro-Engine (ME) to process host data transfer requests for data transfers; and

a doorbell manager arranged to update the context information needed for said Micro-Engine (ME) to process host data transfer requests for data transfers.

11. The host-fabric adapter as claimed in claim 10, wherein said context memory contains a large quantities of context registers arranged to store context information needed for said Micro-Engine (ME) to process said host data transfer requests for data transfers.

12. The host-fabric adapter as claimed in claim 10, wherein said context memory having a bandwidth-optimized, area-minimal vertically sliced memory architecture is partitioned vertically into multiple memory slices based on a register width requirement, each of which supplies respective bits of data of a predetermined register width to said Micro-Engine (ME), via

a system bus of said predetermined register width, and a total number of registers of said multiple memory slices corresponds to a designated number needed by network device requirements.

13. The host-fabric adapter as claimed in claim 10, wherein said context memory having a bandwidth-optimized, area-minimal vertically sliced memory architecture is partitioned vertically into multiple memory slices based on a register width requirement, each of said memory slices contains registers corresponding to a total number of registers provided by data network requirements, each of said memory slices has a register width selected to supply respective bits of data to said Micro-Engine (ME), via a system bus of a predetermined register width, and a register depth selected to correspond to the total number of registers provided, and all of said memory slices except for a last memory slice contain a respective default location initialized to zero which serves as a padding value to said system bus of said predetermined register width, when the respective last memory location of said memory slices is accessed by said Micro-Engine.

14. The host-fabric adapter as claimed in claim 10, wherein said Micro-Engine (ME), said serial interface, said host interface, said context memory, and said doorbell manager are implemented as part of an Application Specific Integrated Circuit (ASIC).

15. The host-fabric adapter as claimed in claim 10, wherein, when a register width requirement is 32 bits, and a system architecture requires 15 registers of 8 bits, 8 registers of 12 bits, and 17 registers of 32 bits for a total of 40 registers, said context memory having a bandwidth optimized, vertically sliced memory architecture is partitioned into three memory slices, including Memory A of 40x8 registers arranged to supply first 8 bits of 32-bit data, via a system bus of 32 bits, Memory B of 25x4 registers arranged to supply next 4 bits of 32-bit data, via said system bus of 32 bits, and Memory Z of 17x20 registers arranged to supply last 20 bits of 32-bit data, via said system bus of 32 bits, wherein said Memory B and Memory Z each contains an additional default, last memory location initialized to zero which serves as a padding value to said system bus of 32 bits, when the respective default, last memory location of a respective memory slice is accessed by said Micro-Engine.

16. The host-fabric adapter as claimed in claim 10, wherein, when a register width requirement is 32 bits and a system architecture requires 5 registers of 8 bits, 10 registers of 12 bits, 15 registers of 24 bits and 20 registers of 32 bits for a total of 50 registers, said context memory having a bandwidth optimized, vertically sliced memory architecture is partitioned into four memory slices, including Memory A of 50x8 registers arranged to supply first 8 bits of 32-bit data, via a system bus of 32 bits, Memory B of 45x4 registers arranged to supply next 4 bits of 32-bit data, via said system bus of 32 bits, Memory C of 35x12 registers arranged to supply next 12 bits of 32-bit data, and Memory Z of 20x8 registers arranged to supply last 8 bits of 32-bit

data, via said system bus of 32-bits, wherein said Memory B, Memory C and Memory Z each contains an additional default, last memory location initialized to zero which serves as a padding value to said system bus of 32 bits, when the respective default, last memory location of a respective memory slice is accessed by said Micro-Engine.

17. A method of designing a context memory having a bandwidth-optimized, area-minimal vertically sliced memory architecture, comprising:

determining a register width requirement and a system architecture requirement of registers of different sizes designated for said context memory;

selecting a number of vertically arranged memory slices of registers of different sizes based on the register width requirement and the system architecture requirement such that each memory slice has a number of registers provided by said system architecture and is arranged to supply respective bits of data, via a system bus of said register width requirement;

determining the depth of each of said memory slices based on the respective number of registers provided by said system architecture; and

establishing a default location that is initialized to zero ("0") in all subsequent memory slices which serves as a padding value when a memory location of a respective memory slice exceeding a register width of said memory slice is accessed, via said system bus.

18. The method as claimed in claim 17, wherein said context memory is arranged to store context information needed for one or more Micro-Engines (MEs) in a host-fabric adapter to process host data transfer requests for data transfers.

19. The process as claimed in claim 17, wherein, when a register width requirement is 32 bits, and a system architecture requires 15 registers of 8 bits, 8 registers of 12 bits, and 17 registers of 32 bits for a total of 40 registers, said context memory having a bandwidth optimized, vertically sliced memory architecture is partitioned into three memory slices, including Memory A of 40x8 registers arranged to supply first 8 bits of 32-bit data, via a system bus of 32 bits, Memory B of 25x4 registers arranged to supply next 4 bits of 32-bit data, via said system bus of 32 bits, and Memory Z of 17x20 registers arranged to supply last 20 bits of 32-bit data, via said system bus of 32 bits, wherein said Memory B and Memory Z each contains an additional default, last memory location initialized to zero which serves as a padding value to said system bus of 32 bits, when the respective default, last memory location of a respective memory slice is accessed by said Micro-Engine.

20. The process as claimed in claim 17, wherein, when a register width requirement is 32 bits and a system architecture requires 5 registers of 8 bits, 10 registers of 12 bits, 15 registers of 24 bits and 20 registers of 32 bits for a total of 50 registers, said context memory having a bandwidth optimized, vertically sliced memory architecture is partitioned into four memory

slices, including Memory A of 50x8 registers arranged to supply first 8 bits of 32-bit data, via a system bus of 32 bits, Memory B of 45x4 registers arranged to supply next 4 bits of 32-bit data, via said system bus of 32 bits, Memory C of 35x12 registers arranged to supply next 12 bits of 32-bit data, and Memory Z of 20x8 registers arranged to supply last 8 bits of 32-bit data, via said system bus of 32-bits, wherein said Memory B, Memory C and Memory Z each contains an additional default, last memory location initialized to zero which serves as a padding value to said system bus of 32 bits, when the respective default, last memory location of a respective memory slice is accessed by said Micro-Engine.